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2.32 kV Breakdown Voltage Lateral β-Ga_2O_3 MOSFETs with Source-Connected Field Plate

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We report on demonstrating high performance lateral β-Ga_2O_3 metal-oxide-semiconductor field-effect transistors (MOSFETs) with source-connected field plate (FP) on a thin (150 nm) and highly Si-doped ($n = 1.5 \times 10^{18}$ cm^{-3}) β-Ga_2O_3 epitaxial channel layer grown by ozone molecular beam epitaxy (MBE) on Fe-doped semi-insulating (010) substrate. For a MOSFET with a gate-drain spacing (L_{gd}) of 25 μm, the three terminal off-state breakdown voltage (V_{BR}) tested in Fluorinert ambient reaches 2321 V. To the best of our knowledge, this is the first report of lateral β-Ga_2O_3 MOSFET with high V_{BR} of more than 2 kV and the highest V_{BR} attained among all the Ga_2O_3 MOSFETs. The breakdown voltages with different L_{gd} from 5–25 μm ranged from 518–2321V, with a linear trend of increasing breakdown voltage for larger spacing lateral MOSFETs. Combining with high electrical performances and excellent material properties, source-connected FP lateral β-Ga_2O_3 MOSFET implies its great potential for next generation high-voltage and high-power switching devices applications above 2 kV.
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Although gallium oxide (Ga_2O_3) exists as different phases of α, β, δ, γ, and ε under various thermodynamic conditions, monoclinic β-Ga_2O_3 is the most stable form with a wide bandgap up to 4.9 eV[1] and a high expected breakdown electric field (E_{BR}) of about 6–8 MV/cm.[2] Thanks to its ultra-wide bandgap (UWBG), it has a wide potential for high electric field,[3–5] high temperature,[6,7] and UV optoelectronics applications.[8,9] Among these advantages of β-Ga_2O_3, the high breakdown electric field (E_{BR}) is the most attractive property. Because the Baliga's figure-of-merit (FOM), which is the basic parameter to evaluate how suitable a semiconductor is for power devices, is proportional to E_{BR}^3, but is only linearly proportional to the mobility (μ). As compared to GaN and SiC, the conduction loss of β-Ga_2O_3 power devices can be one order of magnitude lower at the same breakdown voltage (V_{BR}). Moreover, high quality β-Ga_2O_3 wafers can be manufactured in large volumes by scalable low cost melt-growth techniques.[10] For these reasons, β-Ga_2O_3 is very attractive to use in high-voltage and high-power switching electronics applications such as renewable energy, electric vehicles, defense electronics and power conditioning in large industrial motors.[11,12]

A few high performance Ga_2O_3 power devices have been reported in recent years. They include a vertical Schottky barrier diode (SBD) with high V_{BR} of 2.3 kV,[12] a record high FP lateral SBD with more than 3 kV V_{BR},[13] a high cutoff frequency and maximum oscillation frequency (f_T/f_{max}) of 3.3/12.9 GHz[14] and a record high breakdown field of 3.8 MV/cm[3] and later 5.2 MV/cm.[4] Following the first demonstration of Ga_2O_3 MOSFET with three-terminal off-state V_{BR} of 370V in 2013,[15] a V_{BR} of 382 V with selective SOG doping of source and drain,[16] a recessed enhanced-mode MOSFET with V_{BR} of 505 V,[17] a FP lateral MOSFET with high V_{BR} of 755 kV,[18] a vertical MOSFET with high V_{BR} of 1 kV,[19] and a record high lateral MOSFETs with 1.85 kV V_{BR} by adopting gate-connected field plate and composite dielectrics layers[20] have been reported.

In this work, we report a lateral β-Ga_2O_3 MOSFET with source-connected field plate with a record high V_{BR} of 2321 V. A thin (150 nm) and highly Si-doped (1.5×10^{18} cm^{-3}) β-Ga_2O_3 epitaxial channel layer grown by ozone MBE on Fe-doped semi-insulating (010) β-Ga_2O_3 bulk substrate can achieve the highest experimentally reported V_{BR} in lateral β-Ga_2O_3 FP-MOSFETs. For this device, the E_{BR} is calculated to be 0.93 MV/cm.

Experimental

Most electrical parameters such as pinch-off voltage (V_p), specific on-resistance ($R_{on,sp.}$), I_{on}/I_{off} ratio, current density (A/mm) and V_{BR} of the power MOSFETs are mainly determined by the channel design. Since this is our first device process, we have intuitively determined the epitaxial layer growth method and channel layer design based on the experience of the gallium arsenide (GaAs) power metal-semiconductor field-effect transistors (MESFETs). First, Fe-doped semi-insulating (010) β-Ga_2O_3 substrate and ozone MBE method were used to reduce substrate leakage current during operation of high power MOSFETs and increase the controllability of growth parameters of Si-doped thin β-Ga_2O_3 homoepitaxial channel layer.

In the channel design, we increased the doping concentration to order of 10^{18} cm^{-3} to form ohmic contacts without additional process, such as selective ion implantation with annealing and epitaxial layer regrowth with etching, at source and drain regions to improve ohmic contact properties. On the other hand, the channel layer thickness was reduced to much thinner than those of previous reported devices to decrease the pinch-off voltage of the device. The channel layer thickness (150 nm) and Si donor concentration (1.5×10^{18} cm^{-3}) were verified by electrochemical capacitance-voltage (ECV) measurement as-grown at Novel Crystal in Japan. The Fe-doped semi-insulating (010) substrates used for epitaxial growth were grown by the edge-defined, film fed growth (EFG) method. At the current technology level, the maximum available wafer size is 10 mm × 15 mm and used for device fabrication in this work.

The device fabrication began with a custom-made epi wafer and a monitor of unintentionally doped (UID) Ga_2O_3 piece with same size. A 20 nm Al_2O_3 dielectric was deposited on the Ga_2O_3 free surface before starting process to keep original clean surface as-grown by plasm-enhanced atomic layer deposition (PEALD) at 300°C, which served as both the gate dielectric and channel pre-passivation. Device isolation was carried out with an inductively coupled plasma (ICP) reactive ion etch (RIE) using BCl_3/N_2 mixed gas chemistry. The composition of mixed etch gas was 12.5% N_2 in BCl_3 and the chamber pressure was fixed at 5 mTorr. The RF bias power was adjusted as low as 10% of ICP coil power to reduce plasma particle damage. Under these conditions, the mesa etched angle was about 150 degree, which was suitable for removing disconnection issue of metal lines that cross over the mesa etched channel region. Al_2O_3 layer in the source and drain regions was removed for ohmic metal contact to Ga_2O_3 using buffered

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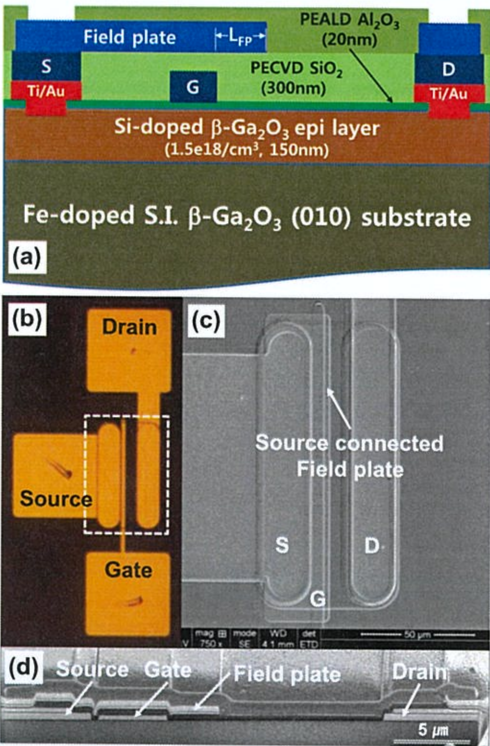

Figure 1. (a) Cross-section view of FP β-Ga_2O_3 MOSFET illustrating the structure of a source-connected FP. (b) Optical microscope of finger-type MOSFET taken after gate electrode formation and basic d.c. parameter measurements. (c) Top-down SEM image and (d) Cross-sectional SEM view of source-connected FP-MOSFET.

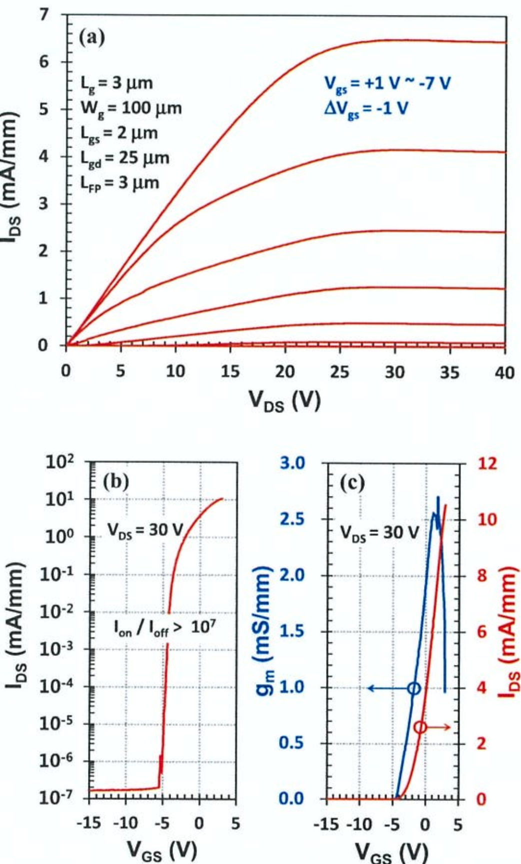

Figure 2. (a) DC Output current-voltage characteristics of the fabricated FP MOSFET with $L_{gd} = 25$ μm. (b) and (c) are semi-log and linear scale transfer characteristics measured at $V_{DS} = 30$ V, along with the extracted I_{on}/I_{off} ratio over 10^7.

oxide solution. Then source-drain ohmic contacts of the transistor were formed by depositing a Ti/Au (25/300 nm) metal layer using an E-beam evaporator and then annealing for 1 minute at 475°C in a nitrogen (N_2) ambient. Circular transmission line method (C-TLM) was used to evaluate metal-semiconductor ohmic contact property. Unlike expectations, specific contact resistivity (ρ_c) was as high as 6.0×10^{-3} $\Omega\cdot cm^2$. So, selective ion implantation and/or epitaxial regrowth process will be tried to improve ohmic contact properties in the next process.

After gate patterning and wafer cleaning with diluted HCl solution, the sample was deposited using a Ti/Au (25/300 nm) metal stack at pressure $< 1 \times 10^{-7}$ Torr. The gate-connected, source-connected, and drain-connected field plates are already well known as FP technologies in lateral GaN-based RF and power devices to increase their breakdown voltages. In particular, at low frequencies, the source-connected FP is more suitable for increasing the uniformity of the electric field profile across gate region and lowering peak electric field at the drain-side edge of the gate in the lateral GaN/AlGaN HEMTs. Because this characteristic might reduce the probability of breakdown at weaker points of the device, a source-connected FP structure, which is different from those of the previous reports, was applied in this work. Source-connected FP length (L_{FP}) was designed to be 3 μm.

After checking the basic device characteristics, a 300 nm SiO_2 field-plate dielectric film was grown by plasm-enhanced chemical vapor deposition (PECVD) at 300°C. This dielectric was used to serve a dual functionality for field-plate mechanical support as well as device surface passivation including mesa etched area. The dielectric via holes were formed by a CF_4-based ICP RIE method and then a thick Ti/Au (20/450 nm) field plate metal was deposited for facilitating pad probing during measurement and reducing electrical resistance of the devices. Finally, all the devices were passivated with a 200nm Si_3N_4 dielectric layer by PECVD and then probing pads were opened by ICP RIE.

A cross-sectional view of β-Ga_2O_3 MOSFET with source-connected FP and MBE-grown epitaxial layers used in this work is shown in Fig. 1a. Three different dielectric films of Al_2O_3, SiO_2, and Si_3N_4 are used for the high voltage device fabrication. The uppermost layer (dark green) of 200 nm Si_3N_4 film is used for final passivation and its description is not shown in this figure. Fig. 1b shows an optical microscope of finger-type MOSFET taken after gate electrode formation and basic d.c. parameter measurements. Fig. 1c shows a top-down SEM image of a lateral MOSFET with source-connected FP structure cross-over the gate finger. This corresponds to the region indicated by the dotted line in Fig. 1b. Device parameters are unit gate width (W_g) of 100 μm, gate length (L_g) of 3 μm, field plate length (L_{FP}) of 3 μm, and gate-drain spacing (L_{gd}) of 5, 10, 15, 20, and 25 μm. Fig. 1d shows cross-sectional SEM view of the source, gate, drain and FP shapes of a source-connected FP-MOSFET with $L_g = 3$ μm, $L_{FP} =$ 3 μm, and $L_{gd} = 15$ μm, obtained from the focused ion beam (FIB) analysis. The L_{gd} and L_{FP}, which mainly affect the breakdown voltage of the device, are formed about 14 μm (~1 μm narrow) and about 3.3 μm (~10% larger), respectively. Since the real L_{gd} value of the device was narrower than that of the designed one, if the E_{BR} calculation is performed based on actual L_{gd}, the E_{BR} values will be higher than those shown in Fig. 4. Therefore, the designed values are used for convenience of calculation of the E_{BR} with the L_{gd} of MOSFETs in this work.

Results and Discussion

DC output current-voltage (I-V) characteristics of the fabricated source-connected FP-MOSFET with $L_g = 3$ μm, $L_{FP} = 3$ μm, and L_{gd} = 25 μm were measured with an HP 4156B semiconductor parameter analyzer on a Cascade probe station at room temperature under air atmosphere conditions and shown in Fig. 2. Fig. 2a shows DC output

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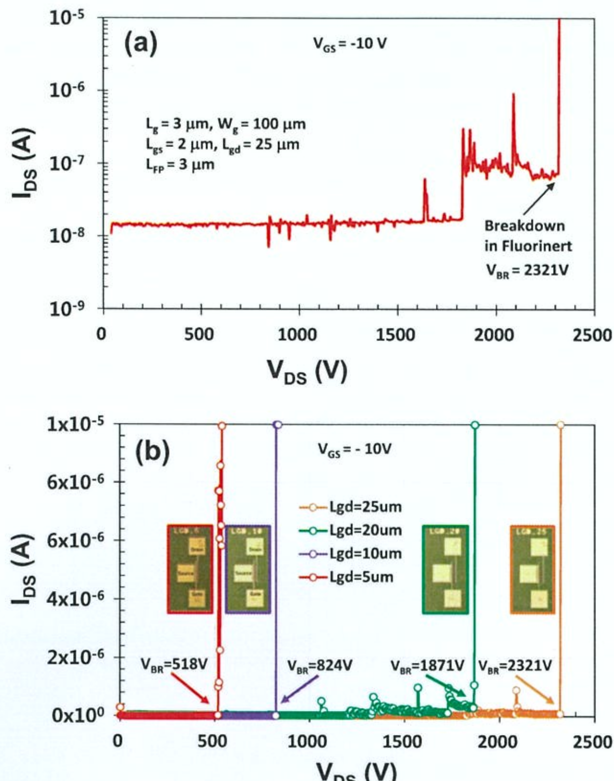

Figure 3. Three-terminal off-state breakdown characteristics of source-connected FP-MOSFETs (a) for L_{gd} = 25 μm in semi-log scale and (b) for L_{gd} = 5 μm, 10 μm, 20 μm, and 25 μm in linear-scale at a constant V_{gs} = −10 V. All breakdown voltages are measured in Fluorinert FC-770 with system compliance of 10 μA, defined as the catastrophic breakdown criteria in this work.

family curves from V_{gs} = + 1 V to V_{gs} = −7 V with a gate voltage step of −1V. Fig. 2b and Fig. 2c show semi-log and linear scale transfer characteristics measured from V_{gs} = + 3 V to V_{gs} = −15 V with a gate voltage step of −0.05 V and at a constant V_{DS} = 30 V, respectively. The I_{on}/I_{off} ratio was estimated as high as 10^7. The pinch-off voltage, which is defined by a drain current density of 100 nA/mm,[3] is typically observed around −4.6 V. The device shows a peak g_m of 2.55 mS/mm at V_{gs} = + 1.3 V. The drain current density at V_{gs} = + 3 V and V_{DS} = 30 V is typically around 10 mA/mm, as shown in Fig. 2b and Fig. 2c.

The three-terminal off-state breakdown characteristics were measured with a Keithley Tektronix 371A High Power Curve Tracer. For the breakdown measurements, the devices were submerged in Fluorinert FC-770 to reduce air breakdown potential. Before breakdown test, we checked the leakage current level of the devices at V_{GS} = −10V and V_{DS} = + 30 V conditions. All leakage current levels of drain and gate were lower than 1.5 × 10^{-8} A. The system compliance was adjusted to 10 μA (∼ × 1000 higher than original leakage current) based on our own reference to protect the system during the catastrophic breakdown of the device and this value was used as a device breakdown criteria. The drain voltage was swept from 0 V to 3 kV with a voltage step of 2 V at a constant V_{gs} = − 10 V. For a device with L_{gd} = 25 μm, the catastrophic breakdown was occurred at 2321 V as shown in Fig. 3a. This is the highest record of V_{BR} measured in a lateral FP Ga_2O_3 MOSFET to date. The V_{BR} for L_{gd} = 5 μm, 10 μm, and 20 μm were also measured with the same criteria of 10 μA and shown with L_{gd} = 25 μm in Fig. 3b.

Figure 4 shows V_{BR} and E_{BR} vs. L_{gd} of the measured devices in this work. The experimental E_{BR} is simply calculated by dividing V_{BR} over L_{gd} as mentioned reason in previous experimental section. The V_{BR} was monotonically increased with L_{gd}. The E_{BR} for a device with

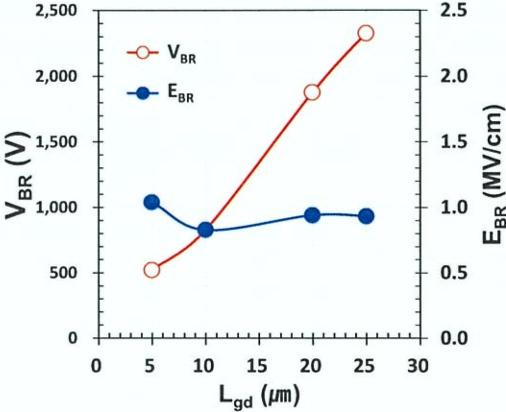

Figure 4. Breakdown voltage V_{BR} and breakdown electric field E_{BR} vs gate-drain spacing L_{gd} in measured devices. The E_{BR} is simply calculated by dividing V_{BR} (from measurement data shown in Fig. 3.) over L_{gd}.

L_{gd} = 25 μm was 0.93 MV/cm and other devices also have values near 1 MV/cm, which is similar with reported data by K. Zeng et al.[20] However this is very low compared to the expected β-Ga_2O_3 E_{BR} of 6 − 8 MV/cm,[2] 3.8 MV/cm for L_{gd} = 0.6 μm,[3] and 5.2 MV/cm for 181 nm-thick β-Ga_2O_3.[4] This means that as the L_{gd} increases, the breakdown occurs at weaker points such as the dielectric films and FP edge rather than the breakdown of the Ga_2O_3 itself. In order to utilize the intrinsic E_{BR} of the Ga_2O_3 channel layer, the dielectric materials used below and above the FP should have large dielectric constant and/or enough thickness.

Figure 5 shows a comparison of $R_{on,sp}$ vs. V_{BR} of device figure of merit (FOM) against previously reported lateral Ga_2O_3 MOSFETs relative to the theoretical limits of Si, GaN and Ga_2O_3. Developed a source-connected lateral β-Ga_2O_3 FP-MOSFET with L_{gd} = 25 μm showed a record high V_{BR} of 2321 V and a $R_{on,sp}$ of 959 Ω·cm². This good result is attributed to the optimization of process conditions of plasma enhanced atomic layer deposition (PEALD) of Al_2O_3 gate dielectric[21] and the passivation schemes with internal SiO_2 and external Si_3N_4 dielectric films by PECVD in the device structure as shown in Fig. 1a. Another device with L_{gd} = 20 μm also showed a high V_{BR} of 1871 V. Previous reported FP β-Ga_2O_3 MOSFET with same L_{gd} = 20 μm showed a high V_{BR} of 1850 V and a $R_{on,sp}$ of about 2100 Ω·cm².[20] Our device shows as high as V_{BR} but very low

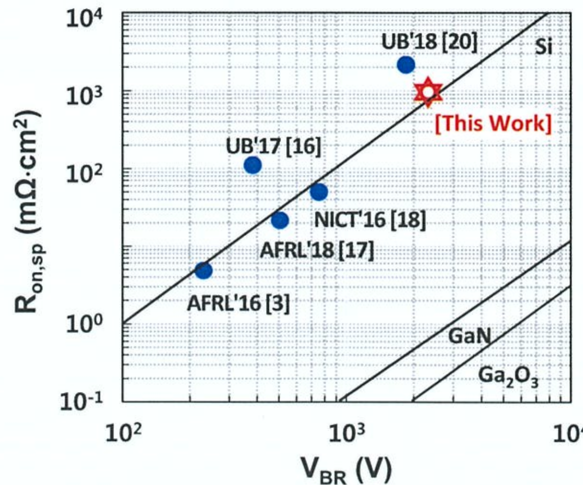

Figure 5. Plot of $R_{on,sp}$ vs. V_{BR} of device figure of merit (FOM) against previously reported lateral Ga_2O_3 MOSFETs relative to the theoretical limits of Si, GaN and Ga_2O_3. $R_{on,sp}$ in this work is calculated by multiplying the active area to the on-resistance ($R_{ds,on}$) of the test device (from the reciprocal slope of I-V curve at V_{GS} = + 1.0 V and V_{DS} = 7 V).

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$R_{on,sp}$. This is due to a high doping concentration (1.5×10^{18} cm^{-3}) of the channel. It is noted that high performance power MOSFETs with low $R_{on,sp}$ and high V_{BR} could be implemented with increasing doping concentration of the thin channel and adopting source-connected FP structure described in this work. In addition to high electrical performances of the Ga_2O_3-based MOSFETs and SBDs and its excellent material properties, the promising low cost and large-size β-Ga_2O_3 substrates produced from melt-grown method as well as the high speed epitaxial layer growth techniques can reduce the whole cost of power devices and hence making it possible for commercial products in near future.[13,22,23]

Conclusions

High performance lateral β-Ga_2O_3 MOSFETs with source-connected field plate are demonstrated on Si-doped thin channel layer grown by MBE on Fe-doped semi-insulating β-Ga_2O_3 bulk substrate. A record-high three-terminal off-state breakdown voltage of more than 2.32 kV is measured in source-connected FP lateral β-Ga_2O_3 MOSFETs with a gate-drain spacing $L_{gd} = 25$ μm and a field plate length $L_{FP} = 3$ μm. The results indicate that source-connected FP lateral β-Ga_2O_3 MOSFETs are very promising candidates for next generation high-voltage and high-power switching devices applications above 2 kV. In conclusion, source-connected FP technology provides a stable, low cost and effective way to make high breakdown voltage in lateral β-Ga_2O_3 MOSFETs.

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