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# Investigation of current collapse and recovery time due to deep level defect traps in $\beta$-$Ga_2O_3$ HEMT

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**Abstract:** In this paper, drain current transient characteristics of $\beta$-$Ga_2O_3$ high electron mobility transistor (HEMT) are studied to access current collapse and recovery time due to dynamic population and de-population of deep level traps and interface traps. An approximately 10 min, and 1 h of recovery time to steady-state drain current value is measured under 1 ms of stress on the gate and drain electrodes due to iron (Fe)–doped $\beta$-$Ga_2O_3$ substrate and germanium (Ge)–doped $\beta$-$Ga_2O_3$ epitaxial layer respectively. On-state current lag is more severe due to widely reported defect trap $E_C$ – 0.82 eV over $E_C$ – 0.78 eV, –0.75 eV present in Iron (Fe)-doped $\beta$-$Ga_2O_3$ bulk crystals. A negligible amount of current degradation is observed in the latter case due to the trap level at $E_C$ – 0.98 eV. It is found that occupancy of ionized trap density varied mostly under the gate and gate–source area. This investigation of reversible current collapse phenomenon and assessment of recovery time in $\beta$-$Ga_2O_3$ HEMT is carried out through 2D device simulations using appropriate velocity and charge transport models. This work can further help in the proper characterization of $\beta$-$Ga_2O_3$ devices to understand temporary and permanent device degradation.

**Key words:** $\beta$-$Ga_2O_3$; current collapse; degradation; HEMT; recovery time; traps; trapping effects

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## 1. Introduction

There has recently been considerable interest in monoclinic $\beta$-phase of gallium oxide ($\beta$-$Ga_2O_3$) inspired by its excellent material characteristics—large energy bandgap $E_G$ ~ 4.9 eV[1], high breakdown electric field $E_{Br}$ up to 8 MV/cm[2], and high electron velocity $v_{sat}$ ~ 1.5 × $10^7$ cm/s[3]. Wide variety of intentional n-type dopants—Si, Ge, and Sn as shallow donors facilitate to achieve electron concentrations ~ 1 × $10^{20}$ $cm^{-3}$[4], although p-type doping in $Ga_2O_3$ shows inconsistent findings[5, 6]. Additionally, with the help of low-cost melt growth techniques, such as Czochralski[7], and floating zone[8], large size $Ga_2O_3$ bulk substrate can be grown and thus offers cost competitiveness over other wideband semiconductors—GaN and SiC. The availability of low cost and large size $\beta$-$Ga_2O_3$ bulk crystalline substrates further enables different epitaxial technologies, such as molecular beam epitaxy (MBE), and halide vapor phase epitaxy (HVPE) to grow $Ga_2O_3$ with low crystal defects on native substrate. To compensate unintentional Silicon (Si) incorporation during growth of $Ga_2O_3$, deep level acceptors such as Mg, and Fe are used to achieve semi insulating bulk crystals[2], and controls substrate leakage. Out of the promising n-type dopants, Si, Ge, and Sn; Ge shows preferred choice for $\beta$-$Ga_2O_3$ devices[4].

Several experimental studies on defects throughout the entire bandgap of $\beta$-$Ga_2O_3$ (010) layers have used deep level transient spectroscopy (DLTS) and deep level optical spectroscopy (DLOS) techniques[9–12]. Three distinct trap states at $w_C$ – 0.1 eV, 0.2 eV, and 0.98 eV in Ge-doped (010) $\beta$-$Ga_2O_3$ grown using plasma assisted MBE[9], $E_C$ – 0.62 eV, 0.82 eV, 1 eV in unintentionally doped (UID) (010) $\beta$-$Ga_2O_3$ using edge-defined film-fed growth (EFG)[10], $E_C$ – 0.55 eV, 0.74 eV, and 1.04 eV[11] in $\beta$-$Ga_2O_3$ crystal grown using Czochralski method, and two deep level traps at $E_C$ – 0.78 eV (due to Fe impurities) and $E_C$ – 0.75 eV (due to intrinsic defect)[12] in upper part of the bandgap with concentrations varying from $10^{14}$ to $10^{16}$ $cm^{-3}$ have been demonstrated.

With the distinct trap level defects reported so far, device performance can be easily questioned unless different trap sources and their individual effects on specific output parameters are fully established because device degradation may be reversible or permanent in nature. Significant progress in $Ga_2O_3$ based electronic devices such as Schottky diodes[13], metal semiconductor FET (MESFET)[2], metal oxide semiconductor FET (MOSFET)[14, 15], modulation doped FET (MODFET)[16], and HEMT[17] have been reported with good DC and RF performance, mainly due to $Ga_2O_3$ excellent material properties. Traps in the device can affect thermal characteristics, including on resistance ($R_{on}$) and threshold voltage ($V_{Th}$), a shift of 0.78 V in $V_{Th}$ was measured due to two distinct trap levels at 0.7 eV, and 0.77 eV in $\beta$-$Ga_2O_3$ MESFETs on Fe-doped $\beta$-$Ga_2O_3$ substrate[18]. Dynamic dispersion in drain characteristics led current lag due to trap at $E_C$ – 0.75 eV was demonstrated in back-gated $Ga_2O_3$ based MOSFET[19].

Potential application of $\beta$-$Ga_2O_3$ based devices beg the question of whether the device degradation due to various traps $E_C$ – 0.98, 0.82, 0.78, 0.75 eV[9, 10, 12] is temporary or per-

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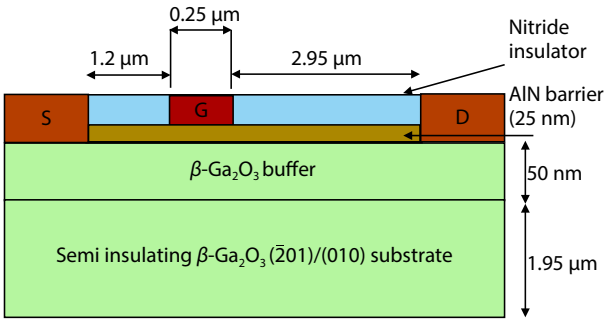


Fig. 1. (Color online) Schematic cross sectional view of the analysed device structure.

manent in nature? In this work, we focus on traps originated from Fe-doped $\beta$-$Ga_2O_3$ substrate, and Ge-doped epitaxial layer on Sn-doped $\beta$-$Ga_2O_3$ substrate to model the reversible current collapse phenomenon along with measurement of current recovery time to its steady state value.

## 2. Device structure and simulation framework

Fig. 1 shows device structure of AlN/$\beta$-$Ga_2O_3$ HEMT which is analysed in this report. The sequence of materials comprise of 25 nm AlN barrier layer on 2 $\mu$m $\beta$-$Ga_2O_3$ substrate. Gate material of Au/Ni with gate length, $L_G$ of 0.25 $\mu$m and Schottky barrier height of 0.8 eV is set by fixing the work function, $\phi_M$ of the gate metal of 2.2 eV, electron affinity of the AlN barrier is set as 1.4 eV[20] in material properties. Source/drain electrodes are considered to be perfectly Ohmic. The gate–source ($L_{GS}$), gate–drain ($L_{GD}$), and source–drain ($L_{SD}$) spacing are 1.2, 2.95, and 4.4 $\mu$m, respectively. Silicon nitride ($Si_3N_4$) insulator of 25 nm is used as surface passivation to suppress current collapse as per experimental device[2].

Using electron and hole effective masses of $\beta$-$Ga_2O_3$[21], total conduction band ($N_C$) and valence band ($N_V$) density of states of $3.6 \times 10^{18}$ and $2.86 \times 10^{20}$ cm$^{-3}$, respectively, were calculated, and other parameters were considered from Ref. [17].

For undoped AlN layer default material parameters as mentioned in Ref. [22] are considered except electron affinity ($\chi$ = 1.4 eV). Due to low in-plane lattice mismatch between AlN/$\beta$-$Ga_2O_3$ heterojunction, spontaneous and piezoelectric polarization built in model[22] is activated for AlN material region. A large conduction band offset (CBO), $\Delta E_C$ = 1.75 eV[20] offers polarization induced sheet charge density $\sigma = 5.617 \times 10^{13}$ C/cm$^2$[23] at the heterointerface due to sole polarization of AlN layer. In absence of p-type carriers, $\beta$-$Ga_2O_3$ based devices are unipolar, so negative differential mobility model as given by Eq. (1) is chosen for $\beta$-$Ga_2O_3$ material region and default values of parameters[22] are replaced by mobility model[3]. The low-field electron mobility of 140 cm$^2$/(V·s) as reported in Ref. [3] is in good agreement with Hall measurements electron mobility of 162 cm$^2$/(V·s)[17].

$$\mu_n(E) = \frac{\mu_{n0} + \dfrac{v_{sat_n}}{E}\left(\dfrac{E}{\mathrm{ECRITN}}\right)^{\mathrm{gamman}}}{1 + \left(\dfrac{E}{\mathrm{ECRITN}}\right)^{\mathrm{gamman}}}. \quad (1)$$

Based on previous published reports[9–12], among the four electron trap levels—$E_1$, $E_2$, $E_3$, and $E_4$; the most prominent is $E_2$ and especially dominant in ($\bar{2}$01) sample, and the source of this trap level is intentional dopant Fe[12]. So to quantify the effect of Fe dopants led current collapse of drain current, the $\beta$-$Ga_2O_3$ substrate is doped with iron (Fe) as acceptor traps with energy level $E_C$ –0.78 eV, and 0.75 eV[12]. The Fe doping in the substrate has a Gaussian profile with peak concentration of $10^{18}$ cm$^{-3}$ at $y$ = 1.0 $\mu$m, and gradually drops to $10^{16}$ cm$^{-3}$ near the surface. In order to analyse the effect of traps, generated by commonly used n-type dopants, Ge in $\beta$-$Ga_2O_3$ epitaxial layer, three trap levels at $E_C$ –0.1 eV, –0.2 eV, –0.98 eV are uniformly doped in 50 nm buffer layer. In this case, the substrate is doped with n-type dopant (Sn) concentration of $10^{18}$ cm$^{-3}$ to minimize the Fe effect in epitaxial layer as demonstrated in Ref. [9]. The state $E_C$ –0.98 eV is also confirmed by Zhang *et al.*[10] as $E_C$ –1.0 eV by DLTS in Ni/$\beta$-$Ga_2O_3$ Schottky diode on unintentional doped (UID) (010) substrate by edge-defined film-fed growth (EFG). All the trap levels are analysed in regard of current collapse phenomenon and are summarized in Table 1 with other characteristics. Only deep level traps with concentration $\geqslant 10^{15}$ cm$^{-3}$ are considered.

## 3. Results and discussions

The proposed device is analysed under three different conditions—gate stress, drain stress, and gate–drain stress. In all three bias conditions, device is biased in low stress and high stress state for 0.1 to 1 ms with respective DC bias at the gate and drain terminals. During initial bias condition, the device is simulated for output drain current under DC bias at gate and drain terminal. After applying a DC bias of $V_{GS}$ = 0 V and $V_{DS}$ = 5 V, this initial bias condition is maintained for 1 ms in dynamic mode. Then, the device is pulsed into high stress state, –25 V on the gate (in gate stress condition); 25 V on the drain terminal (in drain stress); and –25 to 25 V on the gate and drain terminals respectively for another 1 ms, as shown in Fig. 2. Then, the device is returned to its original bias condition. Since we are analysing the recoverable current collapse phenomenon which is not permanent in nature[24], in post-stress condition traps should gradually return to steady state occupancy state. To quantify the recovery time to steady state, bias condition is analysed for a longer time in the order of $10^5$ s in post stress condition. Fig. 3 shows current collapse phenomenon resulting of stress bias, as shown in Fig. 2. The drain current spikes momentarily to its maximum value corresponding to $V_{GS}$ = 0 V and $V_{DS}$ = 25 V and collapses at 2 ms. The trapping of electrons in deep level defects causes this undesirable effect and degrades the device performance.

To analyse the effect of these deep level traps under gate-stress condition, the drain bias remains at fixed bias of 5 V; the device is driven into pinch-off (high stress at gate –25 V for 1 ms) followed by steady state bias. The resulting drain current collapse and recovery time is shown in Fig. 4. It is evident that current degrades momentarily and almost full current recovery happens at time $t$ = 2 ms.

Similar steps are performed to simulate the device under drain stress with appropriate drain and gate bias and the results are shown in Fig. 5. Due to the low concentration ($10^{14}$ cm$^{-3}$) of deep level traps at $E_C$ – 0.1 eV, – 0.2 eV in Ge-doped epitaxial layer there is no current collapse pheno-

Table 1. Deep level traps reported in $\beta$-$Ga_2O_3$ substrate and epitaxial layer, energy level, capture cross section and trap concentration. Fe and Ge enabled current collapse and drain current recovery time to pre-stress condition.

| Reference | Trap energy levels (eV) | Capture cross section ($10^{-14}$ cm$^{-2}$) | Trap source | Trap concentration ($10^{15}$ cm$^{-3}$) | Current collapse/ recovery time |
|---|---|---|---|---|---|
| [12] | $E_C$ – 0.78 | 0.7 | Fe-doped substrate ($\bar{2}01$) | 10 | Moderate/ few seconds |
| | $E_C$ – 0.75 | 5 | Fe-doped substrate ($\bar{2}01$) | 10 | Moderate/ few minutes |
| [9] | $E_C$ – 0.98 | 0.1– 9 | Ge-doped PAMBE on (010) substrate | 1.6 | Mild/ ~ 1 h |
| [10] | $E_C$ – 0.82 | 1 | UID bulk EFG wafer (010) | 36 | Severe/ ~ 10 min |

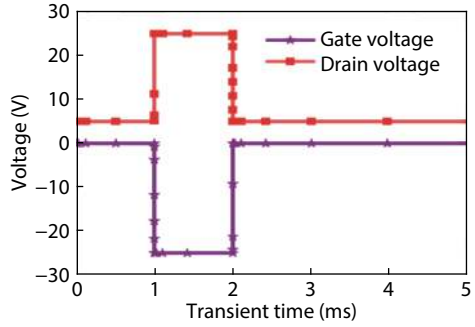


Fig. 2. (Color online) Pre-stress and post-stress bias voltages at gate and drain terminals.

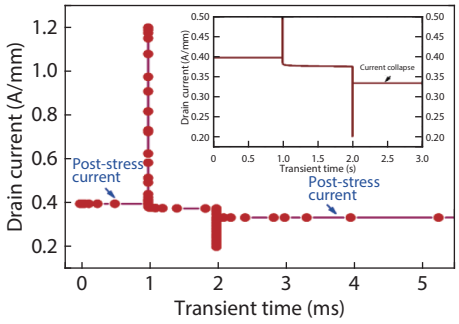


Fig. 3. (Color online) Pre-stress and post-stress drain current. Inset: current collapse.

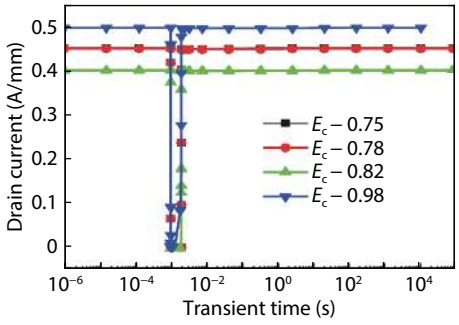


Fig. 4. (Color online) Trapping and de-trapping of defect trap under gate stress.

menon observed. In gate and drain stress bias conditions, both terminals are put in high stress for 1 ms with – 25 V at gate and 25 V at drain terminal. The results are shown in Fig. 6. Current collapse is evident mainly due to traps at $E_C$ –0.82 eV with recovery time of almost 10 min. The trap level at $E_C$ – 0.98 eV demonstrated in Ge-doped epitaxial layer contributes negligibly in current collapse, but steady state drain current restores after a time elapse of 1 h. The other two trap levels $E_C$ – 0.75 eV, 0.78 eV show significant current collapse and recovery time of few seconds to few minutes are quantified respectively, the later one having large capture cross section of $10^{-14}$ cm$^{-2}$.

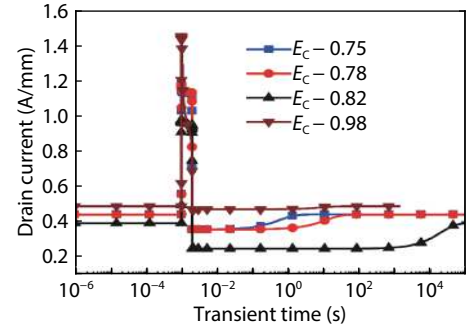


Fig. 5. (Color online) Drain stress and recovery of current recovery due to de-population of traps.

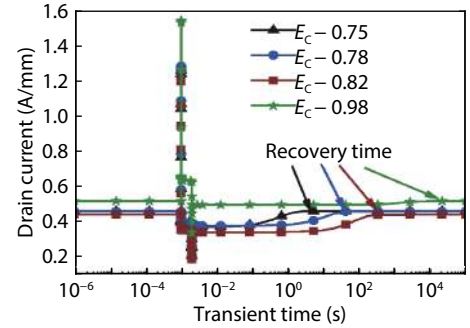


Fig. 6. (Color online) Current collapse and recovery curve, showing intentional doped Fe causes most of the current collapse and Ge doping caused current collapse takes approximately 2 h to attain steady state value.

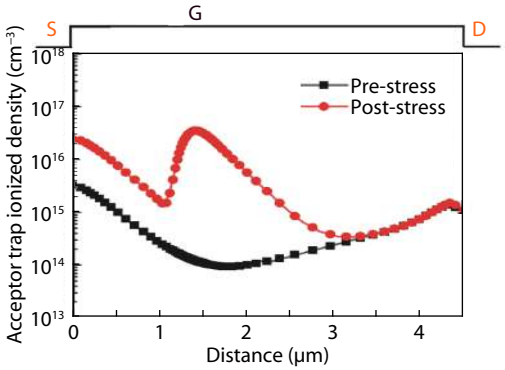


Fig. 7. (Color online) Ionised trap density horizontally at a depth of 0.5 $\mu$m in the substrate.

The ionized Fe trap occupancy before and after high stress bias condition highlights are shown in Fig. 7. It can be seen that the trap density under the gate and gate source area near the surface mostly affects the current degradation. Ionization trap density is plotted at a depth of 0.5 $\mu$m from the surface in the $\beta$-$Ga_2O_3$ substrate. There is a significant

difference in the occupancy of trap along the depth in the substrate and along the horizontal direction towards gate. The gate length of the analysed device, $L_G$ of 0.25 $\mu$m, and the effect of Fe trap occupancy extends along the depth up to 0.5 $\mu$m (two times of gate length), and along source and drain regions. Source, gate, and drain electrodes are shown in upper part of Fig. 7 to correlate device dimension with ionized trap density in the substrate.

## 4. Conclusion

The trapping effects led current collapse phenomenon using drain transient characteristics of $\beta$-$Ga_2O_3$ HEMT is presented. The recovery time for the drain current to return to its steady state value is investigated using Atlas TCAD simulations. The trap level at energy $E_C$ – 0.8 eV in Fe-doped $\beta$-$Ga_2O_3$ substrate plays crucial role in undesirable current collapse phenomenon and the recovery time is about 10 min. In the Ge-doped $\beta$-$Ga_2O_3$ epitaxial layer, the trap level at $E_C$ – 0.98 eV insignificantly degrades the drain current but takes roughly 1 h to restore the original value. This current degradation is reversible event and current returns to its steady state value but only after a finite time varying from few seconds to several minutes depending on the trap characteristics. It is also observed that unintentional interface traps have a negligible effect on current collapse. The report thoroughly establishes that intentional Fe-doping in semi insulating $\beta$-$Ga_2O_3$ substrate led traps cause current collapse, and on the other side recovery time in current lag in Ge-doped $\beta$-$Ga_2O_3$ epitaxial layer is approximately 1 h. By measuring the current recovery time, this report effectively distinguishes between temporary and permanent device degradation due to current collapse. The findings of this work may be useful in reliability study of $\beta$-$Ga_2O_3$ devices.

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