Field-Plated Lateral Ga_2O_3 MOSFETs With Polymer Passivation and 8.03 kV Breakdown Voltage

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***Abstract*— This letter reports the polymer passivation of field plated lateral β-Ga_2 O_3 MOSFETs with significant improvement in the breakdown voltages as compared to non-passivated devices. We show consistent results of higher breakdown voltages in passivated devices as compared to non-passivated devices for MOSFETs with L_{gd} ranging from 30μm to 70μm and across two process runs. We obtain a record high breakdown voltage of 6.72 kV for a MOSFET with $L_{gd} = 40\mu$m giving an average field strength of 1.69 MVcm^{-1}. The peak drain current is $\sim$ 3 mA/mm for $L_g = 2\mu$m device with a gate source separation of 3μm. The on-resistance for the device is, R_{on} = 13 kΩ·mm, giving a power device Figure of Merit of 7.73 kWcm^{-2}. The R_{on} is high due to plasma induced damage of channel and access regions. The R_{on} and on-current density remain unchanged after passivation. The breakdown increases with L_{gd} up to 70μm, giving a maximum breakdown voltage of 8.03 kV.**

***Index Terms*— Gallium oxide, field plate, passivation layer, breakdown voltage, fluorinert, electron device.**

I. Introduction

β-GALLIUM oxide (β-Ga_2O_3) has demonstrated tremendous potential for next generation power devices. This is due to the ultra-wide bandgap of β-Ga_2O_3 (4.5−4.9eV), resulting in high electric field density of $\sim$ 8MVcm^{-1}. A good electron mobility gives a high Baliga's Figure of Merit (BFoM) [1]–[4]. Several groups have reported kV class breakdown voltages and high power device Figure of Merit in Ga_2O_3 devices including lateral MOSFETs [5]–[12], FIN type vertical MOSFETs [13], and Schottky diodes [14]–[18]. In addition, good RF performance [19] and high current densities have also been reported [20]. Recently, triple implant vertical MOSFETs with both depletion and enhancement mode operations have been demonstrated [21]. Although impressive, the breakdown voltages are still far from the estimated breakdown voltages with high critical field strength.

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Previously, it was shown that the parasitic air arcing led to low breakdown voltages in lateral devices and use of Fluorinert significantly improved the breakdown voltage [5], [6]. Moreover, breakdown characteristics with very little increase in currents up to breakdown voltage suggested an extrinsic breakdown mechanism outside the channel. The breakdown voltage scaled with gate-drain spacing with a field strength that is comparable to the Fluorinert field strength [5]. In addition, the temperature dependent breakdown voltage [6] gave a negative temperature coefficient which suggests an extrinsic phenomenon. Intrinsic breakdown mechanism in semiconductors will have a positive co-efficient due to the efficient energy dissipation of accelerated electrons by higher phonon occupancy at higher temperatures [22].

In this letter, we report a SU-8 polymer passivation scheme of field plated lateral Ga_2O_3 MOSFETs. The higher field strength of the SU-8 polymer leads to a significant increase in breakdown voltage at a given gate-drain separation. The passivation layer does not have any adverse effect on input and output I-V characteristics of the devices. For lateral field plated MOSFETs, we report record non-passivated and passivated breakdown voltages of 2.7 kV and 6.72 kV respectively for L_{gd} = 40 μm. For SU-8 passivated device, the measured average field strength (E_{br}) is 1.69 MVcm^{-1}, with simulated peak field of $>$ 10 MVcm^{-1}. In addition, we report a continuous trend of increased V_{br} for passivated devices up to L_{gd} of 70 μm with a high breakdown voltage of 8.03 kV. These reported breakdown voltages are higher than previously reported V_{br} values for Ga_2O_3 devices and higher than reported V_{br} in lateral devices in other wide-bandgap semiconductors [23]–[25].

II. Fabrication and Measurements

A cross-section device schematic is depicted in Figure 1 (a). The device structure and process flow are similar to the previous reports [5], [6]. The epitaxial structure is grown using Molecular Beam Epitaxy (MBE) by Novel Crystal Technology, Inc., Japan, on Fe doped (010) Ga_2O_3 substrates. The channel layer is 200 nm thick with a target Si doping of $\sim$ 6.0 $\times$ 10^{17} cm^{-3}. The top most ohmic layer is 50 nm thick with a target high Si doping of $\sim$ 2.2 $\times$ 10^{19} cm^{-3}. Device fabrication started with photolithographic patterning of source/drain (S/D) contacts followed by electron-beam deposition of 240 nm thick Ti/Au/Ni metal stack. After deposition, S/D contacts underwent rapid thermal annealing at 520 ^{o}C to make the contacts ohmic. Next, the n^{+} layer was removed in a timed RIE in BCl_3/Ar chemistry stopping on the channel.

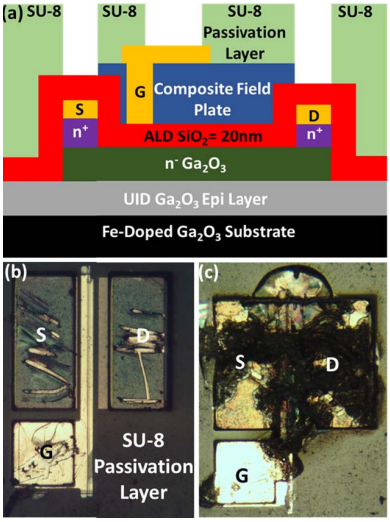

Fig. 1. (a) Device schematic. (b) Optical microscope image of L_{gd} = 30 μm MOSFET. (c) Optical microscope image of MOSFET after breakdown.

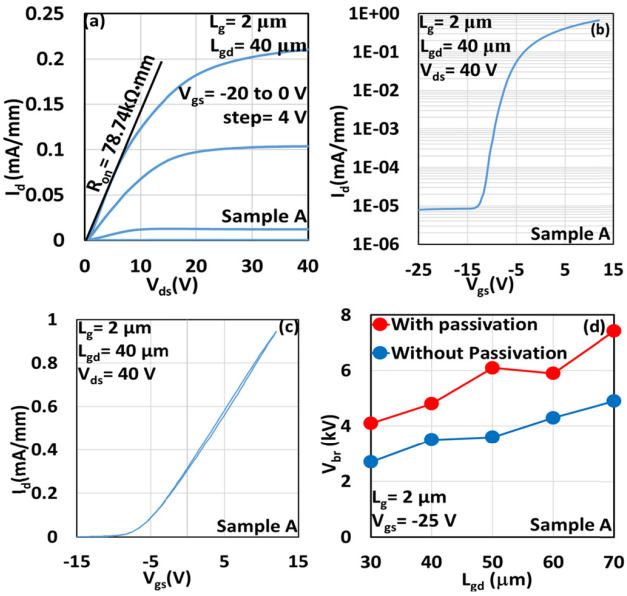

Fig. 2. (a) DC output characteristics and (b) DC input characteristics at V_{ds} = 40 V for L_{gd} = 40 μm MOSFET after SU-8 passivation. (c) DC input characteristics with double sweep. (d) Comparison of V_{br}(kV) with L_{gd} varying from 30 μm to 70 μm. The breakdown measurements were performed with a gate bias of −25 V. All the devices have L_g = 2 μm and L_{sg} = 3μm. **(Sample A)**

Subsequently, a second BCl_3/Ar RIE was done to isolate the devices. Approximately 450 nm of composite ALD/PECVD/ALD oxide layer was deposited, including the bottom gate oxide, which is same as the previous reports [5], [6]. Gate patterning was done following the same procedure as in [5], [6]. The last step in fabrication was device passivation.

To compare the effectiveness of the passivation, device current-voltage characteristics and breakdown voltages were measured before SU-8 passivation. The SU-8 passivation followed the standard recommended process [26]. After spin coating and baking, SU-8 was patterned to open the source/drain and gate pads. The SU-8 was then hard-baked at 200 °C for 10 minutes. An optical micrograph of the fabricated device with SU-8 passivation layer is shown in Fig. 1 (b). The device input and output characteristics were measured using HP 4155B semiconductor parameter analyzer. The breakdown characteristics were measured using Keysight B1505A power device analyzer with Keysight N1268A Ultra High Voltage (UHV) expander. The breakdown measurements were carried out with devices submerged in Fluorinert FC-40, even for SU-8 passivated devices, to rule out any air arcing. An optical micrograph of the passivated device after breakdown measurement is shown in Fig. 1 (c).

Two separate device runs (labeled Sample A and Sample B) were carried out to check the effectiveness of passivation scheme. For Sample A, the channel thickness after recess etch was 140 nm, while Sample B had a 190 nm channel after recess etch. The isolation thickness was different for the two samples. Sample A was etched to a thickness of 350 nm from the top of the n^+ ohmic layer, while Sample B was etched to 500 nm. In addition, for Sample A, the device isolation etch was performed before self-aligned etch of the n^+ ohmic cap layer.

III. Results and Discussion

All the devices reported here have a gate length (L_g) of 2 μm and gate-source separation (L_{sg}) of 3 μm. The input and output characteristics of L_{gd} = 40μm device are shown in Fig. 2 (a) and (b) respectively for Sample A. The device has high ON/OFF ($\sim 10^5$) ratio but an order lower on-current density than previous reports [5], [6]. The low current density is due to over-etching of the channel layer in the timed-etch process. The thinner channel layer and the RIE induced damage increased the device resistance. The TLM data gave a very high sheet resistance of 1 MΩ/□ . I-V characteristics did not show any change with SU-8 passivation. Low hysteresis was observed in the device as seen in Fig. 2 (c). The measured breakdown voltage as a function of gate-drain separation is shown in Fig. 2 (d). An increase in breakdown voltage is clearly seen at each gate-drain separation. The improvement can be as high as 2.5 kV as seen in the device with L_{gd} = 50μm. The non-linear increase in breakdown voltage with and without passivation is due to process variation in our samples.

Fig. 3 (a) and (b) show the input and output characteristics of L_{gd} = 40μm device in Sample B with thicker channel. The device has higher ON/OFF ratio ($\sim 10^7$) than Sample A due to the thicker isolation mesa depth. We see a significant improvement in on-state current ($\sim$ 3 mA/mm) compared to Sample A due to the thicker channel layer. Although, the current is higher than Sample A, it is lower compared to previous reports by our group [5], [6]. The lower current is again attributed to the process damage arising from RIE and O_2 plasma treatments used during the fabrication. The TLMs show a high sheet resistance of 53 kΩ/□ . The current drop was observed after the isolation step (not shown) when O_2 plasma was used to clean the sample. A vacuum annealing scheme can recover the damage and improve the current density as reported in [27]. Use of ion-implantation or source regrowth techniques can also significantly increase the current and reduce R_{on}. Low gate hysteresis was observed in the transfer characteristics as seen in Fig. 3 (c).

The measured breakdown characteristics of a representative 40 μm L_{gd} device, with and without SU-8 passivation, are shown in Fig. 3 (d) at V_{gs} = −25 V. The non-passivated

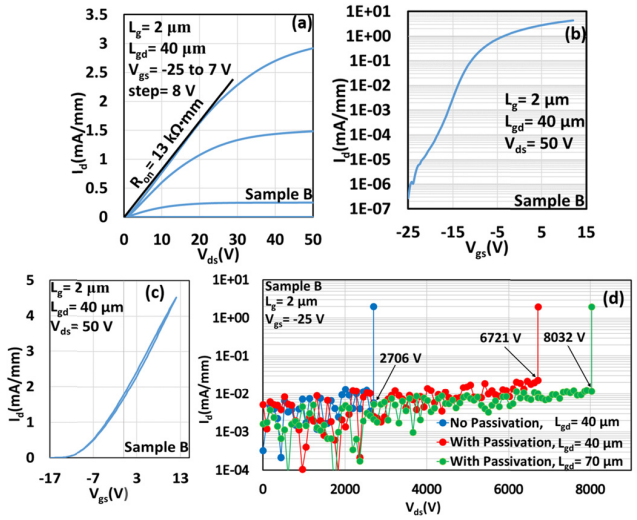

Fig. 3. (a) DC output and (b) input characteristics at V_{ds} = 50 V for L_{gd} = 40 μm MOSFET after passivation. (c) DC input characteristics with double sweep. (d) Breakdown characteristics of L_{gd} = 40 μm device with and without passivation. Also shown is the highest V_{br} for L_{gd} = 70 μm device, 8032V. The breakdown measurements were performed with a gate bias of −25 V. All the devices have L_g = 2 μm and L_{sg} = 3 μm. **(Sample B)**

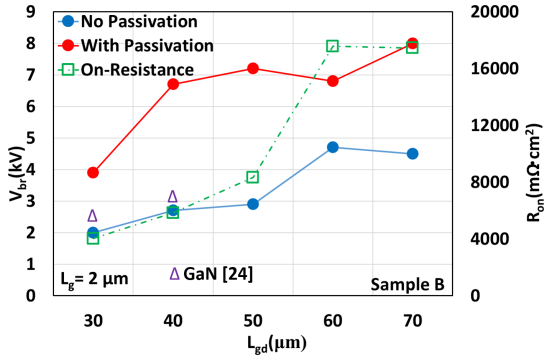

Fig. 4. Comparison between V_{br} and R_{on} of non-passivated and passivated MOSFETs with L_{gd} varying from 30 μm to 70 μm. R_{on} is normalized with $W_g \times L_{sd}$. **(Sample B)**. The reference data is for GaN devices [24].

device showed a breakdown at 2.7 kV, while the passivated device with ∼10 μm thick SU-8 layer showed impressive improvement with a breakdown voltage of 6721 V. It is noted that the baseline leakage current is higher than previous reports [5], [7] due to the increased background leakage current in the Keysight N1268A UHV system. Both devices show a hard-destructive breakdown. For the passivated SU-8 device, an average field strength of 1.69 MVcm^{-1} was calculated. The calculated power device Figure of Merit is 7.73 kWcm^{-2}.

For both Samples A and B, we see a consistent trend of passivated devices showing higher breakdown voltages as compared to non-passivated devices for increasing L_{gd} as seen in Fig. 2(c) and Fig. 4. Thus, it can be attributed to higher dielectric strength of SU-8 (4.4MVcm^{-1}) [28] as compared to the field strength of Fluorinert FC-40, 0.18 MVcm^{-1}. At L_{gd} = 70μm, we report a record high breakdown voltage of 8032 V (Fig. 3 (d)). These breakdown voltages are higher than any previous reports of breakdown voltages in Ga_2O_3 devices and lateral MOSFETs in any semiconductors [23]–[25] with comparable L_{gd}. They show the potential of Ga_2O_3 for beyond 10 kV rating power devices.

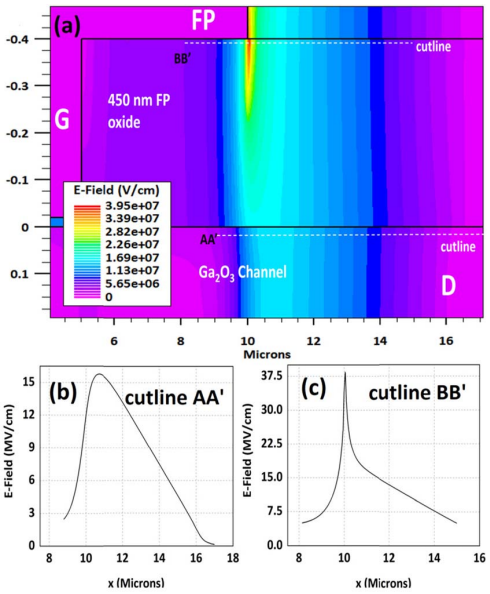

Fig. 5. (a) Silvaco ATLAS simulation of electric field profile for L_{gd} = 40 μm MOSFET with 6.7 kV drain bias. (b) Field in the Ga_2O_3 channel across cutline AA'. (c) Field in the field plate oxide along cutline BB'.

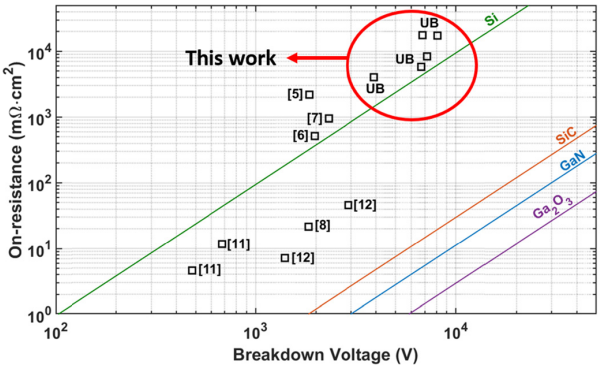

Fig. 6. R_{on} vs Breakdown Voltage plot of lateral Ga_2O_3 MOSFETs from this study and previously reported research. R_{on} is normalized with $W_g \times L_{sd}$.

An ATLAS SILVACO simulation of the L_{gd} = 40μm device at V_{ds} = 6.7 kV shows that very high fields are present both in the field plate oxide and in the Ga_2O_3 channel (> 10 MV/cm). In addition, high field is also present in the gate oxide. Any of these locations can lead to the breakdown. More comprehensive studies are necessary to confirm the breakdown location in these devices. Fig. 6 shows a comparison of the devices in this study with recently reported lateral Ga_2O_3 MOSFETs.

IV. Conclusion

A field-plated Ga_2O_3 MOSFET with polymer passivation is fabricated, demonstrating improvement in breakdown voltage for two samples. The peak on-current density for a L_{gd} = 40 μm device, is ∼ 3 mA/mm, giving a high R_{on} of 13 kΩ. mm. This can be further improved by vacuum annealing. Room temperature breakdown voltage for L_{gd} = 40 um is 6.72 kV, the highest reported for lateral MOSFETs. High R_{on} is indicative of depletion of carrier layers due to etching. R_{on} can be improved by mitigating etch induced depletion. Passivation continued to increase breakdown voltage for devices with L_{gd} up to 70 μm up to 8.03 kV.

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